

Keynote Speaker:

Prof. T. Srinivasulu
DEAN, Kakatiya University

Resource Persons:

Dr. Bhaskar Dudem
RATI, University of Surrey, UK

Prof. P. S. Srinivasa Babu
Department of ECE, K L University



Sri Mamidi Naga Raju
Application Engineer, Entuple Technologies

Sri Kedarnadh
Application Engineer, Entuple Technologies

Sri Sudhir
Application Engineer, Entuple Technologies

Sri Saraswati
Design Engineer, Entuple Technologies

Registration fee:-

Scholars / Researchers : Rs. 500/-
Industry Persons : Rs. 1000/-

Venue :-

Dr. Y. R. Haragopal Reddy Seminar Hall
ECE & EEE Block, Dr.YSR ANUCET

Registration link:-

<https://forms.gle/qHpgYqJcmkkzSgBm7>
Contact: +91-7981752840
email: drbsnagakishore@gmail.com



Dr YSR ANU College of Engineering and Technology
Acharya Nagarjuna University

**UGC Sponsored
National Seminar on
Emerging Trends in VLSI**

28th & 29th March 2022

Registration Form

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Dr. YSR ANU COLLEGE OF ENGINEERING AND TECHNOLOGY
ACHARYA NAGARJUNA UNIVERSITY



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National Seminar on
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Seminar Director

Dr. S Naga Kishore Bhavanam
Asst. Professor & Coordinator, Dept. of ECE

Organized by

Department of Electronics & Communication Engineering
Dr.YSR ANU College of Engineering and Technology
Acharya Nagarjuna University
Nagarjuna Nagar, Guntur, Andhra Pradesh

In Collaboration

AP State Council of Science & Technology
APSCHE Planning and Monitoring Board
Guntur Cluster

About Dr YSR ANUCET

Dr YSR ANU College of Engineering & Technology was established in the academic year 2009 -2010 at Acharya Nagarjuna University campus. It was started with an aim of imparting technical values in the students, who can change the shape of global scenario in engineering arena and also to educate students for careers of leadership, innovation in engineering and its related fields.

Dr. YSR ANUCET secured 601-800 Rank in "World University Ranking by Subject 2022: Engineering" by TIMES HIGHER EDUCATION announced in London. Dr. YSR ANUCET attained 601-800 Rank in Worldwide. 52 Indian Universities got ranked in world wide. Among 52 Universities from INDIA, Dr. YSR ANUCET secured 10th Place. In AP bagged 1st place.

About ECE Department

The department of Electronics and Communication Engineering was established in 2009 with an intake of 60 students in B.Tech. The department has introduced the M.Tech. PG programme with the specialization of Communication Engineering and Signal Processing in 2011 and enrolled Ph.D. in 2010. The programme ensures that the student effectively meets the highest benchmarks of competence required by the industry. Since its establishment, the department has been recognized all over the world for excellence in research environment with active research groups in the areas of Antennas, VLSI, Digital Image Processing, Internet of Things, Networking and Signal Processing.



About Seminar

VLSI stands for "Very Large Scale Integration". This is the field which involves packing more and more logic devices into smaller and smaller areas. Thanks to VLSI, circuits that would have taken board full of space can now be put into a small space few millimetres across! There is a rising demand for chip driven products in consumer electronics, medical electronics, communication, aero-space, computers etc. as no one has space or patience to carry and manage bulky machines. More and more chip designing companies have set up their units in India eyeing on the Indian talents; besides many of the Indian Major IT companies have forayed in Application Specific Integrated Circuit (ASIC) design in a big way. With the design & manufacturing market (both domestic & international) expanding rapidly, there is an enhanced demand of trained professionals who will boost the technical work force in the VLSI domain.

Topics to be covered

Overview of VLSI Design Flow, Tools and Methodology. Latest trends in ASIC Design and EDA tools. Overview of Analog and Digital IC Design flow. Industry standard state-of-art Cadence EDA Solutions. Demo Design for Full Custom-IC Flow using Cadence EDA tools. (10T-SRAM IC Design). Latest trends in Digital IC Design and Cadence EDA tools. Simulation, Synthesis and Physical design flow. Physical Implementation that includes Floor Planning, Power Planning, Placement, CTS, Routing. Demo Design for Semi Custom-IC Flow using Cadence EDA tools (UART Design). Semiconductor Market Trends and Opportunities. Opportunities for Research in VLSI Design.

Research Topics

- Flexible Electronics
- Flexible & Wearable Battery-Free Triboelectric Sensors.

Chief Patron:

Prof. Raja Sekhar Patteti

Vice-Chancellor, ANU

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